50 Hz to 6 GHz 50 dB TruPwr™ Detector

Preliminary Technical Data

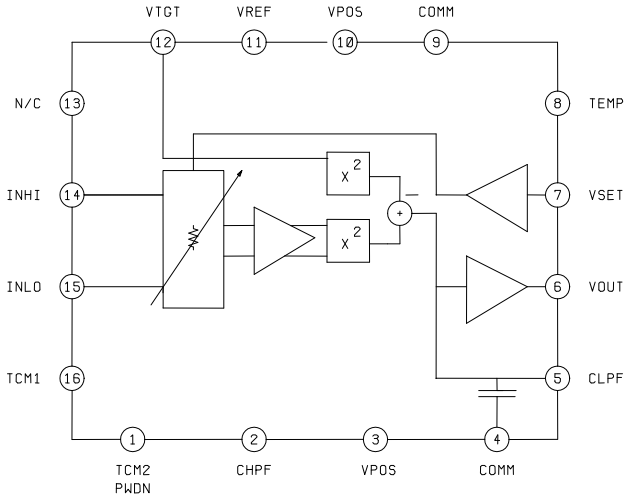
AD8363

FEATURES

Accurate RMS-to-DC conversion from 50 Hz to 6 GHz
Single ended input dynamic range of >50 dB
Waveform and modulation independent, such as WiMAX/GSM/CDMA/WCDMA/TDMA
Linear-in-decibels output, scaled 50 mV/dB
Log conformance error of <0.3 dB
Temperature stability of <±0.5 dB
Voltage supply range of 4.5 V to 5.5 V
Operating temperature range of –40°C to +125°C
Power-down capability

APPLICATIONS

Power amplifier linearization/control loops
Transmitter power controls
Transmitter signal strength indication (TSSI)
RF instrumentation



FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The AD8363 is a true RMS responding power detector that has more than 50 dB measurement range when driven with a single-ended 50 Ω source. The device provides a solution in a variety of high frequency communication systems, and in instrumentation, requiring an accurate response to signal power. The AD8363 is easy to use with its single-ended 50 Ω input, only requiring a single 5 V supply, and a few capacitors. The AD8363 can operate from arbitrarily low frequencies to 6 GHz and can accept inputs that have RMS values from less than -50 dBm to at least 0 dBm, with large crest factors, exceeding the requirements for accurate measurement of WiMAX, WCDMA, and CDMA signals.

The AD8363 can determine the true power of a high frequency signal having a complex low frequency modulation envelope, or can be used as a simple low frequency RMS voltmeter. The high-pass corner generated by its internal offset-nulling loop can be lowered by a capacitor added on the CHPF pin.

Used as a power measurement device, VOUT is connected to VSET. The output is then proportional to the logarithm of the RMS value of the input. In other words, the reading is presented directly in decibels and is conveniently scaled 1 V per decade, or 50 mV/dB; other slopes are easily arranged. In controller mode, the voltage applied to VSET determines the power level required at the input to null the deviation from the set point. The output buffer can provide high load currents.

The AD8363 has 1.5 mW power consumption when powered down by a logic high applied to pin 1, TCM2. It powers up within about 30 µs to its nominal operating current of 60 mA at 25°C. The AD8363 is supplied in a 4 mm x 4 mm, 16-lead LFCSP for operation over the temperature range of –40°C to +125°C. An evaluation board is available.

Rev. PrB

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SPECIFICATIONS

Pins 3, 10 - VPOS = V_S = 5 V, T = 25°C, Z_O = 50 Ω, Single ended input drive, VOUT tied to VSET, VTGT = 1.4, CLPF= 3.9 nF, CHPF=2.7 nF, Error referred to best-fit line (linear regression), unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Maximum Input Frequency			6		GHz
RF INPUT INTERFACE	Pins INHI, INLO, ac-coupled				
Input Impedance	Single-ended drive		50/TBD		Ω/pF
Common Mode Voltage			2.7		V
100 MHz	Pin 16 - TCM1=0.47V, Pin 1 - TCM2= 1.0V				
Output Voltage: High Power in	P_{IN} = -10 dBm		2.48		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.93		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C		62		dB
Maximum Input Level, ±1.0 dB			8		
Minimum Input Level, ±1.0 dB			-54		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.5		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		±0.6		dB
Logarithmic Slope			51.8		mV/dB
Logarithmic Intercept			-58		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
Input Impedance	Single-ended drive		50/TBD		Ω/pF
900 MHz	TCM1= 0.48V, TCM2= 1.2V				
Output Voltage: High Power in	P_{IN} = -10 dBm		2.5		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.91		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C		52		dB
Maximum Input Level, ±1.0 dB			-2		
Minimum Input Level, ±1.0 dB			-54		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		± 0.5		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		± 0.7		dB
Logarithmic Slope			51.9		mV/dB
Logarithmic Intercept			-57.5		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
Input Impedance	Single-ended drive		50/TBD		Ω/pF
1900 MHz	TCM1=0.51V, TCM2= 0.51V				
Output Voltage: High Power in	P_{IN} = -10 dBm		2.38		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.8		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C		42		dB
Maximum Input Level, ±1.0 dB			-10		
Minimum Input Level, ±1.0 dB			-52		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		± 0.5		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		± 0.6		dB
Logarithmic Slope			52		mV/dB
Logarithmic Intercept			-55		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB

Parameter	Conditions	Min	Typ	Max	Unit
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
Input Impedance	Single-ended drive		50/TBD		Ω/pF
2140 MHz	TCM1=0.49V, TCM2=1.2V				
Output Voltage: High Power in	P_{IN} = -10 dBm		2.31		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.72		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C		40		dB
Maximum Input Level, ±1.0 dB			-10		
Minimum Input Level, ±1.0 dB			-50		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		±0.6		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		±0.5		dB
Logarithmic Slope			52.5		mV/dB
Logarithmic Intercept			-53.5		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
Input Impedance	Single-ended drive		50/TBD		Ω/pF
2600 MHz	TCM1=, TCM2=				
Output Voltage: High Power in	P_{IN} = -10 dBm		2.15		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.52		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		35		dB
Maximum Input Level, ±1.0 dB			-12		
Minimum Input Level, ±1.0 dB			-40		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		TBD		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		TBD		dB
Logarithmic Slope			53.2		mV/dB
Logarithmic Intercept			-49.9		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
Input Impedance	Single-ended drive		50/TBD		Ω/pF
3.8 GHz	TCM1=0.56V, TCM2=1.0V				
Output Voltage: High Power in	P_{IN} = -15 dBm		2.0		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.5		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C,		33		dB
Maximum Input Level, ±1.0 dB			-16		
Minimum Input Level, ±1.0 dB			-49		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		+/- 1.0		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		+/- 0.8		dB
Logarithmic Slope			54.7		mV/dB
Logarithmic Intercept			-50		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
5.8 GHz	TCM1=0.88V, TCM2= 1.0V				
Output Voltage: High Power in	P_{IN} = -20 dBm		1.5		V
Output Voltage: Low Power in	P_{IN} = -40 dBm		0.35		V
±1.0 dB Dynamic Range	CW input, T_A = +25°C		30		dB

Parameter	Conditions	Min	Typ	Max	Unit
Maximum Input Level, ±1.0 dB			-17		
Minimum Input Level, ±1.0 dB			-47		
Deviation vs. Temperature	Deviation from output at 25°C				
	-40°C < T_A < +85°C; P_{IN} = -10 dBm		± 0.6		dB
	-40°C < T_A < +85°C; P_{IN} = -40 dBm		± 0.7		dB
Logarithmic Slope			54.5		mV/dB
Logarithmic Intercept			-47		dBm
Deviation from CW Response	13 dB peak-to-rms ratio (WCDMA), over 40 dB dynamic range		±0.1		dB
	12 dB peak-to-rms ratio (WiMAX), over 40 dB dynamic range		±0.1		dB
	14.0 dB peak-to-rms ratio (16C CDMA2K), over 40 dB dynamic range		±0.1		dB
	256 QAM CF=8		±0.1		dB
OUTPUT INTERFACE	Pin 6 - VOUT				
Output Swing					
	Voltage Range Min RL≥200 to ground		.09		v
	Voltage Range Max RL≥200 to ground		Vs-.15		V
	Source/Sink Current Out held at Vs/2K, to 1%change		10		mA
SETPOINT INPUT	Pin VSET				
Voltage Range	Log conformance error ≤1 dB, Min 2140 MHz		TBD		V
	Log conformance error ≤1 dB, Max 2140 MHz		TBD		
Input Resistance			72		kΩ
Logarithmic Scale Factor	f = 2140MHz, −40°C ≤ T_A ≤ +85°C		19		dB/V
Logarithmic Intercept	f = 2140 MHz, −40°C ≤ T_A ≤ +85°C, referred to 50 Ω		−TBD		dBm
TEMPERATURE COMPENSATION	Pin 16 - TCM1, Pin 1 - TCM2				
Input Voltage Range		0		2.5	V
Input Resistance	TCM2		>1		MΩ
	TCM1		3		3kΩ
VOLTAGE REFERENCE	Pin 11 - VREF				
Output Voltage	RF in = −55 dBm		2.3		V
Current Limit Source/Sink	1% change		5/0.08		mA
TEMPERATURE REFERENCE	Pin 8 TEMP				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		1.35		V
Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, R_L ≥ 10 kΩ		4.8		mV/°C
POWER-DOWN INTERFACE	Pin TCM2 (Pin1)				
Logic Level to Enable	Logic LO enables Max		< Vs -.9		V
Logic Level to Disable	Logic HI disables Min		Vs -.8		V
Input Current	Logic HI TCM2 = 5 V		<1		µA
	Logic LO TCM2 = 0 V		<1		µA
Enable Time	TCM2 LO to OUT at .5 dB of final value, C_{LPF} = 470 pF, C_{HPF} = 220 pF, RF in = 0 dBm		30		µs
Disable Time	TCM2 HI to OUT at 10% final value, C_{LPF} = 470 pF, C_{HPF} = 220 pF, RF in = 0 dBm		20		µs
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		4.5	5	5.5	V
Quiescent Current	25C RF in =-55 dBm		60		mA
	+85 C		72		mA
Supply Current	When disabled		310		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage VPOS	5.5 V
Input Power (Into Input of Device)	23 dBm Evaluate
Equivalent Voltage	2 V rms
Internal Power Dissipation	500 mW
θ_{JA}	125°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

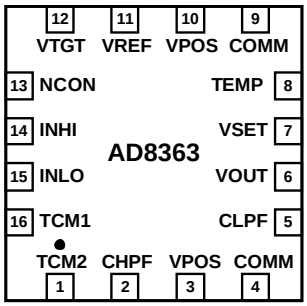


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TCM2/PWDN	A dual function pin used for controlling the amount of nonlinear intercept temperature compensation and/or shutting down the device. This pin can be connected to the VREF pin through a voltage divider if the shut down function is not used
2	CHPF	Connect to VPOS via a capacitor to determine -3 dB point of the input signal high-pass filter.
3, 10	VPOS	Supply for the device. Connect to +5 V power supply.
4, 9	COMM	System Common Connection. Connect via low impedance to system common.
5	CLPF	Connection for Loop Filter Integration (Averaging) Capacitor. Connect a ground-referenced capacitor to this pin. A resistor may be connected in series with this capacitor to improve loop stability and response time.
6	VOUT	Output pin in Measurement Mode (error Amplifier output). In measurement mode, normally connected directly to VSET. This pin can be used to drive a gain control when the device is used in controller mode.
7	VSET	The voltage applied to this pin sets the decibel value of the required RF input voltage that results in zero current flow in the loop integrating capacitor pin, CLPF. The controls the VGA gain such that a 50mV change in VSET reduces the gain by approximately 1dB.
8	TEMP	Temperature Sensor Output.
11	VREF	General-Purpose Reference Voltage Output of 1.16 V.
12	VTGT	Voltage applied to this pin determines the target power at the input of the RF squaring circuit. The intercept voltage is proportional to the voltage applied to this pin. The use of a lower target voltage increases the crest factor capacity; however, this may affect the system loop response.
13	NCON	Not connected.
14	INHI	Single-ended RF input pin. RF input signal is normally AC coupled to this pin through a coupling capacitor.
15	INLO	Grounded for single ended input
16	TCM1	Connect to VREF through a voltage divider or an external DC source. Is used to adjust Intercept temperature compensation (3K impedance)
	Paddle	Connect via low impedance to system common

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, Z_O = 50 Ω, Single ended input drive, VOUT tied to VSET, VTGT = 1.4V, CLPF= 3.9 nF, CHPF=2.7 nF, T_A = +25°C (Black), –40°C (Blue), +85°C (red)

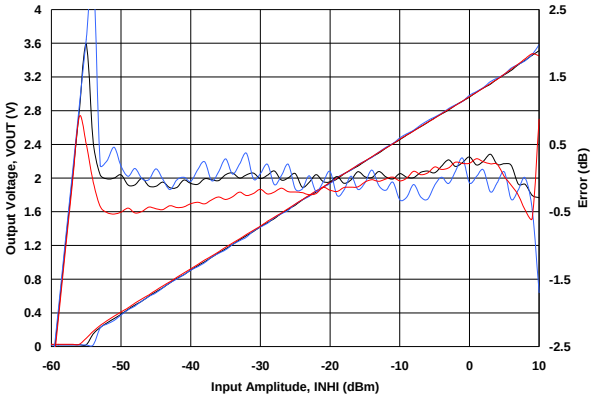


Figure 3. VOUT Voltage and Log Conformance vs. Input Amplitude at 100 MHz, Typical Device, TCM1 = 0.47 V, TCM2 = 1.0 V, Sine Wave, -40C, 25C, 85C

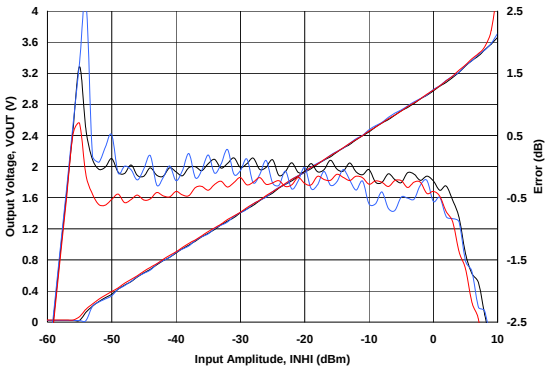


Figure 4. VOUT Voltage and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device, TCM1 = 0.48 V, TCM2 = 1.2 V, Sine Wave -40C, 25C, 85C

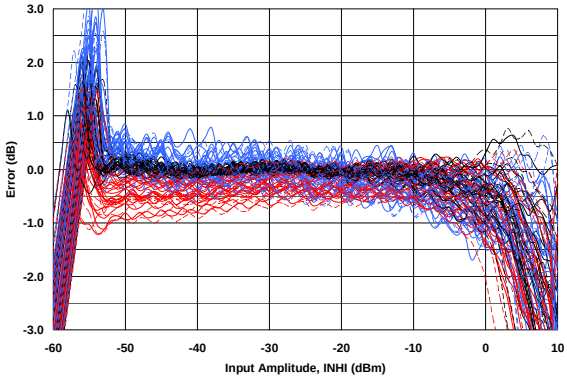


Figure 5. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30 Devices from Multiple Lots, Frequency =900 MHz, TCM1 = 0.48 V, TCM2 = 1.2 V, Sine Wave-40C, 25C, 85C

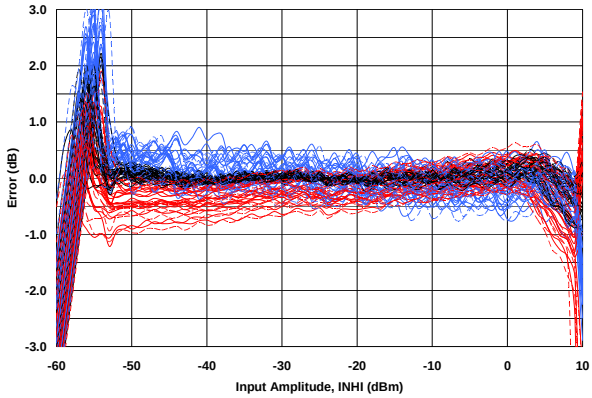


Figure 6. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 30Devices from Multiple Lots, Frequency = 100 MHz, TCM1 = 0.47 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

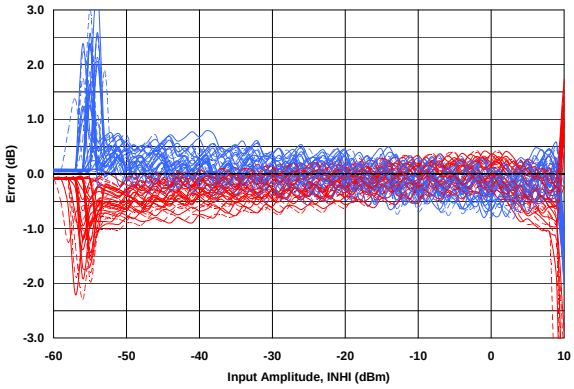


Figure 7. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 30Devices from Multiple Lots, Frequency = 100 MHz, TCM1 = 0.47 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

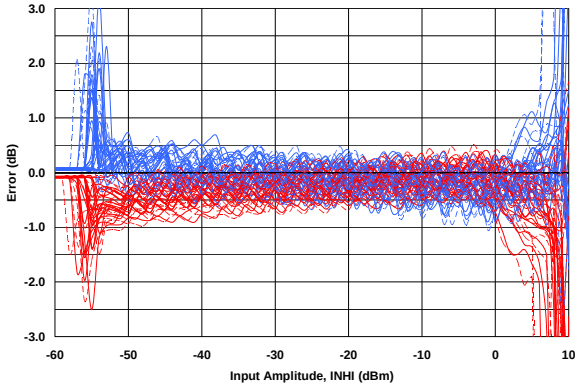


Figure 8. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 30Devices from Multiple Lots,, Frequency =900 MHz, TCM1 = 0.48 V, TCM2 = 1.2 V, Sine Wave-40C, 25C, 85C

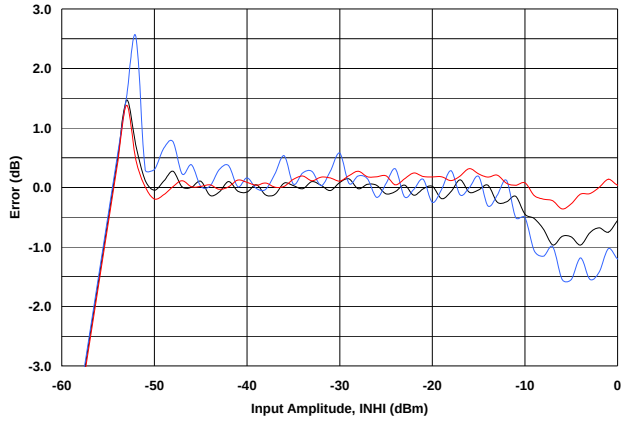


Figure 9. VOUT Voltage and Log Conformance vs. Input Amplitude at 1.90 GHz, Typical Device, TCM1 = 0.51 V, TCM2 = 0.51 V, Sine Wave, -40C, 25C, 85C

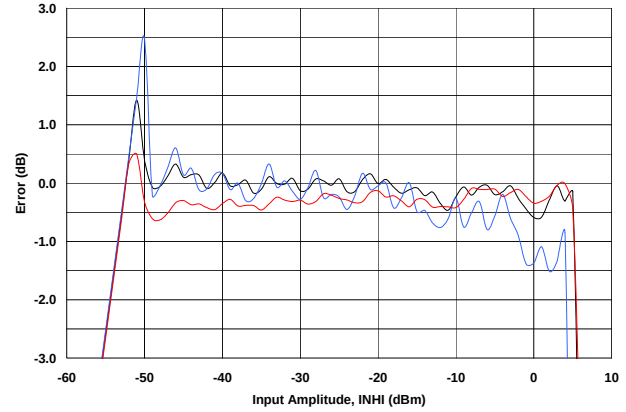


Figure 10. VOUT Voltage and Log Conformance vs. Input Amplitude at 2.14 GHz, Typical Device, TCM1 = 0.49 V, TCM2 = 1.2 V, Sine Wave, -40C, 25C, 85C

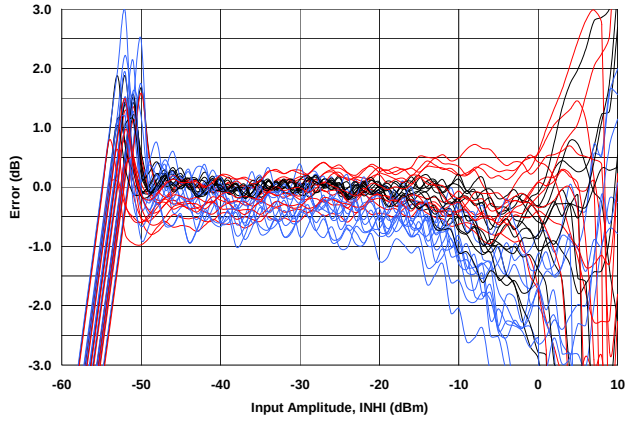


Figure 11. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 18Devices from Multiple Lots, Frequency = 2.14 GHz, TCM1 = 0.49 V, TCM2 = 1.2 V, Sine Wave-40C, 25C, 85C

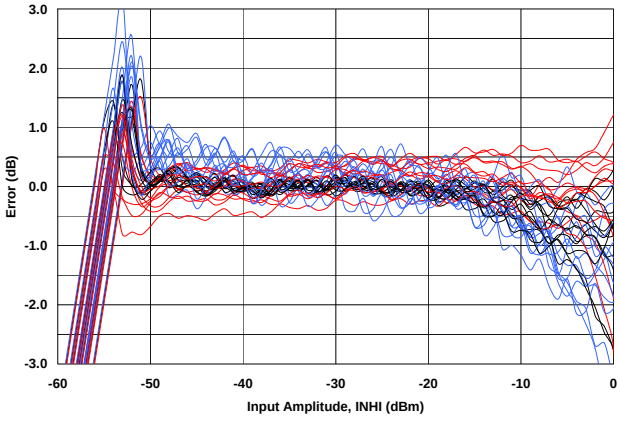


Figure 12. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 18Devices from Multiple Lots, Frequency = 1.9 GHz, TCM1 = 0.51 V, TCM2 = 0.51 V, Sine Wave-40C, 25C, 85C

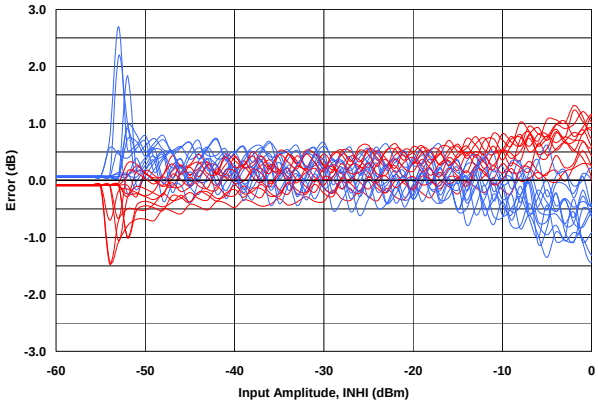


Figure 13. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 18 Devices from Multiple Lots, Frequency = 1.9 GHz, TCM1 = 0.51 V, TCM2 = 0.51 V, Sine Wave-40C, 25C, 85C

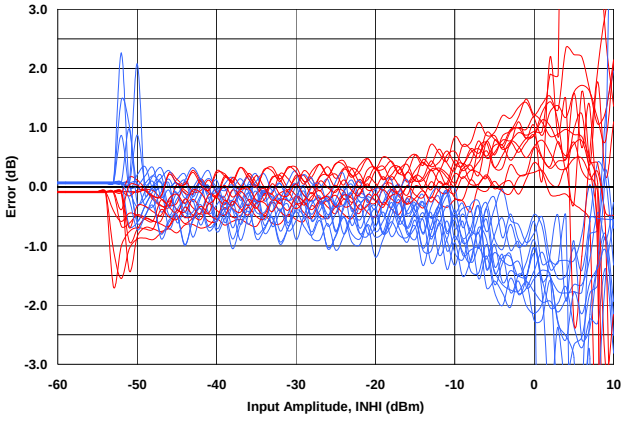


Figure 14. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 18 Devices from Multiple Lots, Frequency = 2.14 GHz, TCM1 = 0.49 V, TCM2 = 1.2 V, Sine Wave-40C, 25C, 85C

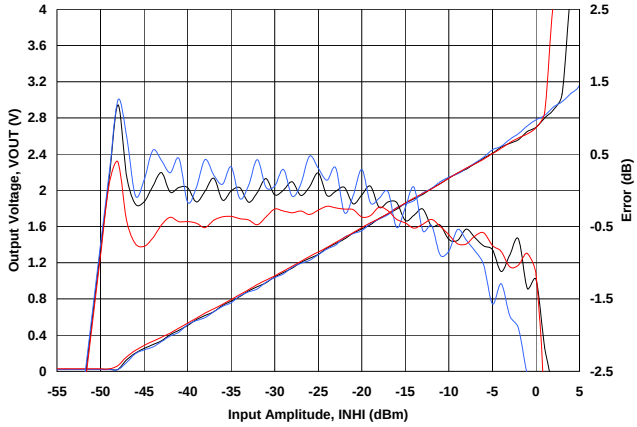


Figure 15. VOUT Voltage and Log Conformance vs. Input Amplitude at 2.6 GHz, Typical Device, TADJ = TBD V, Sine Wave-40C, 25C, 85C

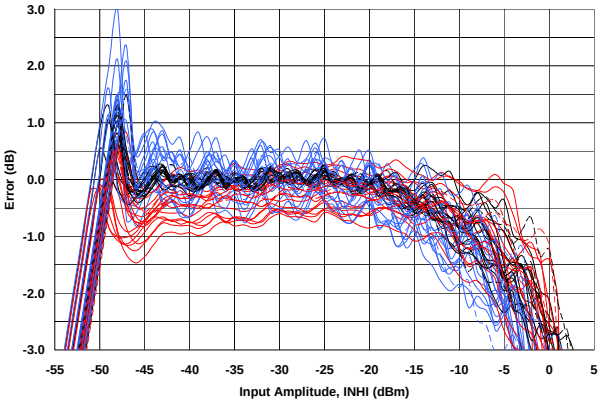


Figure 18. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 17 Devices from Multiple Lots, Frequency = 2.6 GHz, TCM1 = 0.52 V, TCM2 = 1.1 V, Sine Wave-40C, 25C, 85C

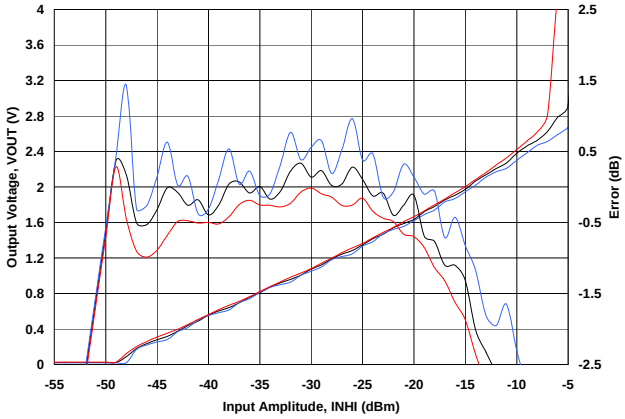


Figure 16. VOUT Voltage and Log Conformance vs. Input Amplitude at 3.8 GHz, Typical Device, TCM1 = 0.56 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

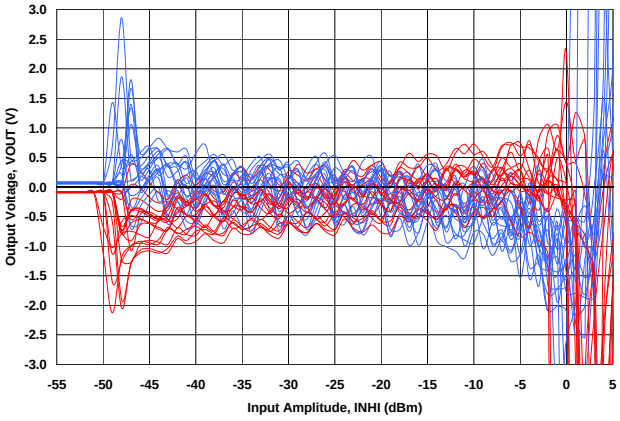


Figure 19. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 17 Devices from Multiple Lots, Frequency = 2.6 GHz, TCM1 = 0.52 V, TCM2 = 1.1 V, Sine Wave-40C, 25C, 85C

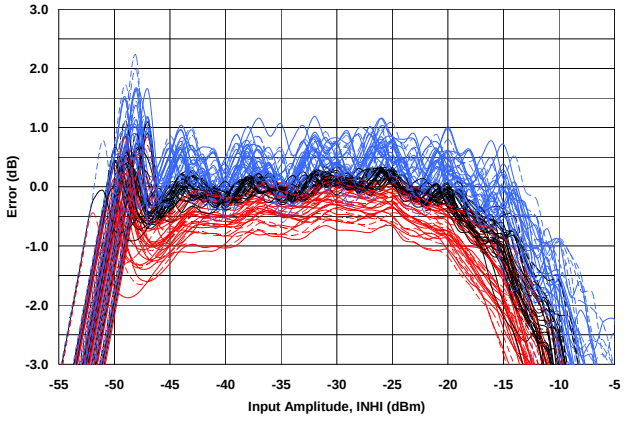


Figure 17. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 37 Devices from Multiple Lots, Frequency = 3.8 GHz, TCM1 = 0.56 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

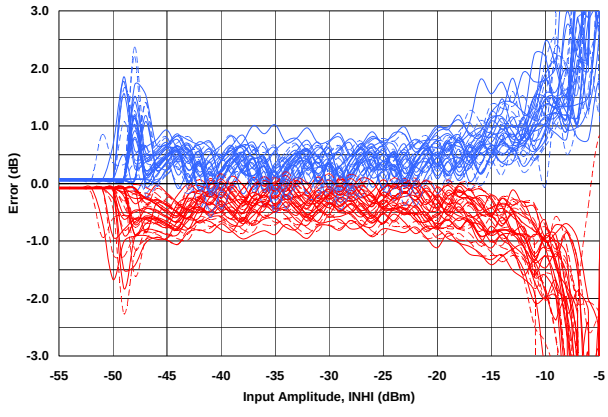


Figure 20. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 37 Devices from Multiple Lots, Frequency = 3.8 GHz, TCM1 = 0.56 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

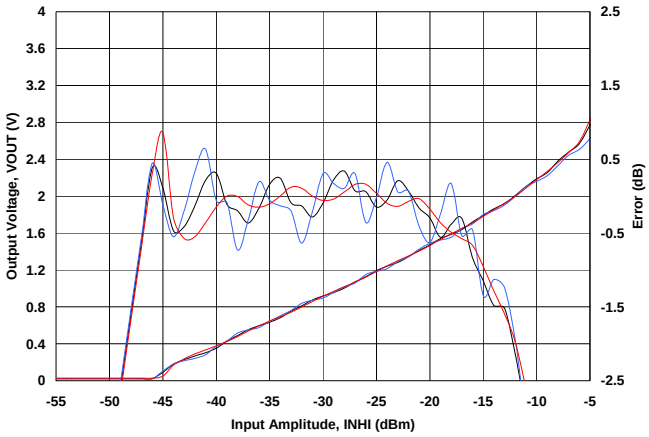


Figure 21. VOUT Voltage and Log Conformance vs. Input Amplitude at 5.8 GHz, Typical Device, TCM1 = 0.88 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

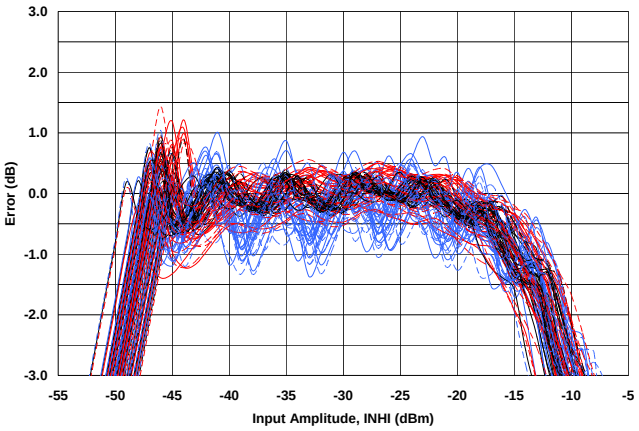


Figure 24. Distribution of VOUT Voltage and Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 37 Devices from Multiple Lots, Frequency = 5.8 GHz, TCM1 = 0.88 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

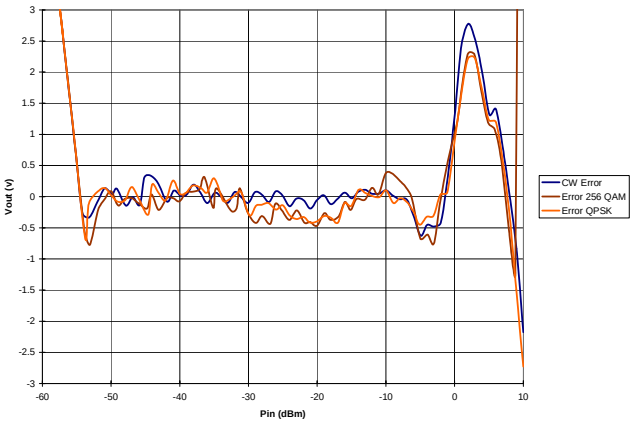


Figure 22. Error from CW Linear Reference vs. Input Amplitude with Different Waveforms, 256 QAM, QPSK, Frequency 2140 MHz

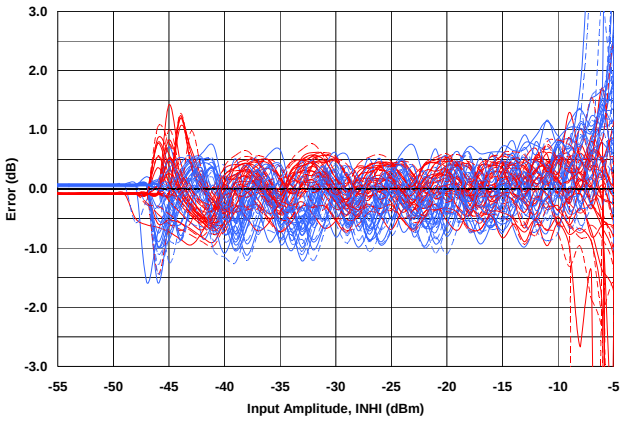


Figure 25. Distribution of Error over Temperature After Ambient Normalization vs. Input Amplitude, with reference to 25C, for at Least 37 Devices from Multiple Lots, Frequency = 5.8 GHz, TCM1 = 0.88 V, TCM2 = 1.0 V, Sine Wave-40C, 25C, 85C

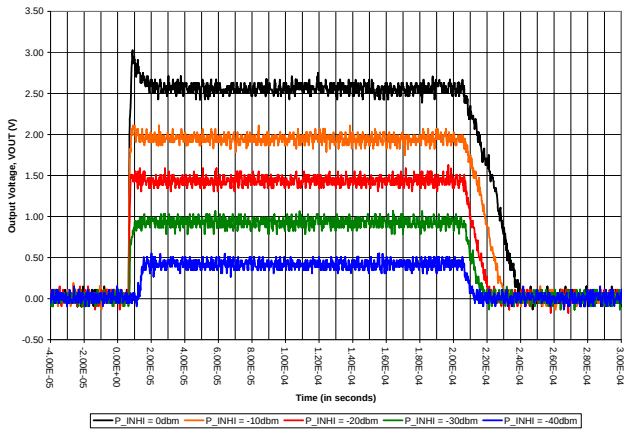


Figure 23. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency 2.14 GHz, CLPF = 470 pF, CHPF=220pF

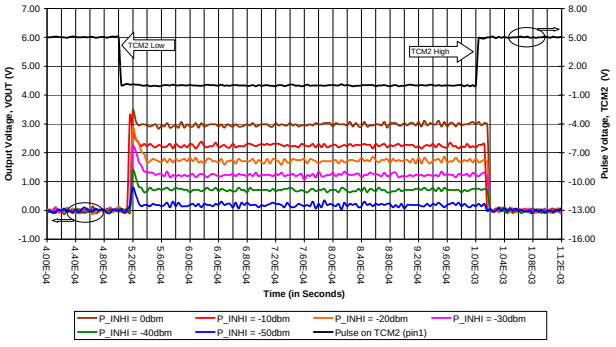


Figure 26. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency 2.14 GHz, CLPF= 470pF, CHPF = 220pF

Table 4. Pin Function Descriptions

Component	Function/Notes	Default Value
C6, C10, C11, C12	Input: The AD8363 was designed to be driven single ended. At frequencies below 2.6 GHz, more dynamic range can be achieved by driving Pin 14 (INHI). In order to do this, C10 and C12 should be populated with an appropriate valued capacitor for the frequency of operation. C6 and C11 should be left open. For frequencies above 2.6 GHz, greater dynamic range can be achieved by Driving Pin 15 (INLO). This can be done by using an appropriate valued capacitor for C6 and C11, while leaving C10 and C12 open.	*C10=0.1uF,* C12=0.1uF, C6=Open, C11=Open
R7, R10, R11	VTGT: R10 and R11 are set up to provide 1.4V to VTGT from VREF. An external voltage can be used if R10 and R11 are removed.	R10=845Ω, R11= 1.4KΩ
C4, C5, C7, C13, R14, R16	Power Supply Decoupling: The nominal supply decoupling consists of a 100 pF filter capacitor placed physically close to the AD8363, a 0 Ω series resistor, and a 0.1 uF capacitor placed closer to the power supply input pin. The 0 Ω resistor can be replaced with a larger value resistor to add more filtering, at the expense of a voltage drop.	C4=100 pF, C5=100 pF, C7= 0.1uF, C13= 0.1uF, R14= 0 Ω, R16= 0 Ω
R1, R2, R6, R13, R15	Output Interface--Measurement Mode: In measurement mode, a portion of the output voltage is fed back to the VSET pin via R6. The magnitude of the slope at VOUT can be increased by reducing the portion of V_{OUT} that is fed back to VSET, using a voltage divider created by R6 and R2 . If a fast responding output is expected, the 0 Ω resistor on R15 can be removed to reduce parasitics on the output. Output Interface--Controller Mode: In this mode, R6 must be open and R13 must have a 0 Ω resistor. In controller mode, the AD8363 can control the gain of an external component. A setpoint voltage is applied to the VSET pin, the value of which corresponds to the desired RF input signal level applied to the AD8363 RF input. If a fast responding output is expected, the 0 Ω resistor on R15 can be removed to reduce parasitics on the output.	R1=0 Ω, R2=Open, R6=0 Ω, R13 = Open , R15 = 0 Ω
C9, C8, R5	Low-pass filter capacitors: The low-pass filter capacitors reduce the noise on the output and affect the pulse response time of the AD8363. The smallest CLPF capacitance should be 400 pF	C8=Open, C9=0.1uF, R5=0 Ω
C3	CHPF capacitor The CHPF capacitor introduces a high-pass filter effect into the AD8363 transfer function and can affect the response time. It should be tied to VPOS.	C3= 2700 pF
R9, R12	TCM2/PWDN: The TCM2/PWDN pin controls the amount of nonlinear intercept temperature compensation and/or shuts down the device. The evaluation board is configured to control this from a test loop but VREF can be used through a voltage divider created from R9 and R12.	R9= Open, R12= Open
R17, R18	TCM1: TCM1 controls the intercept temperature compensation (3K impedance). The evaluation board is configured to control this from a test loop but VREF can be used through a voltage divider created from R17 and R18	R17=Open, R18=Open
Paddle	The paddle should be tied to both a thermal and electrical ground	

EVALUATION BOARD

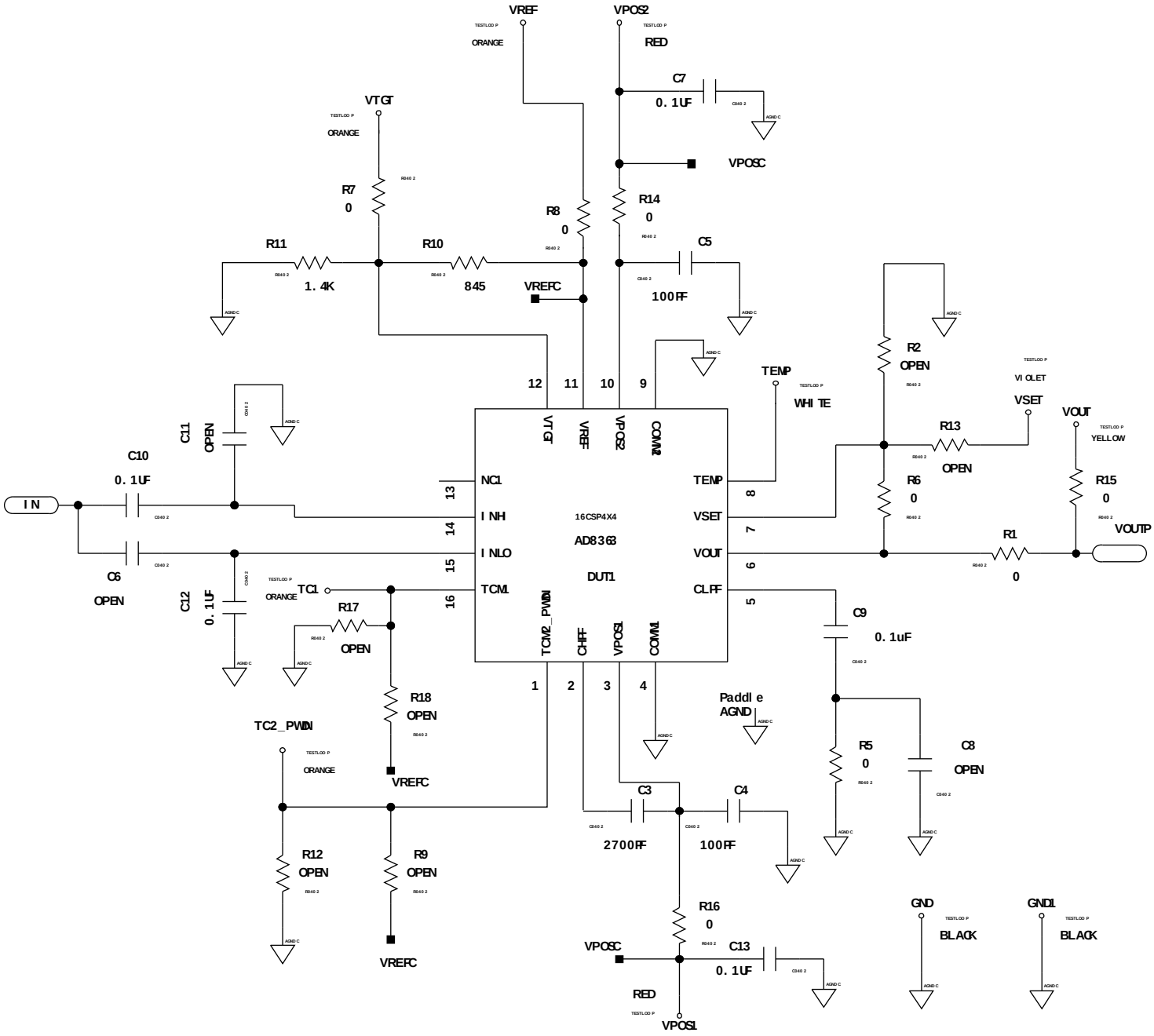


Fig 27 Evaluation Board Schematic

ASSEMBLY DRAWINGS

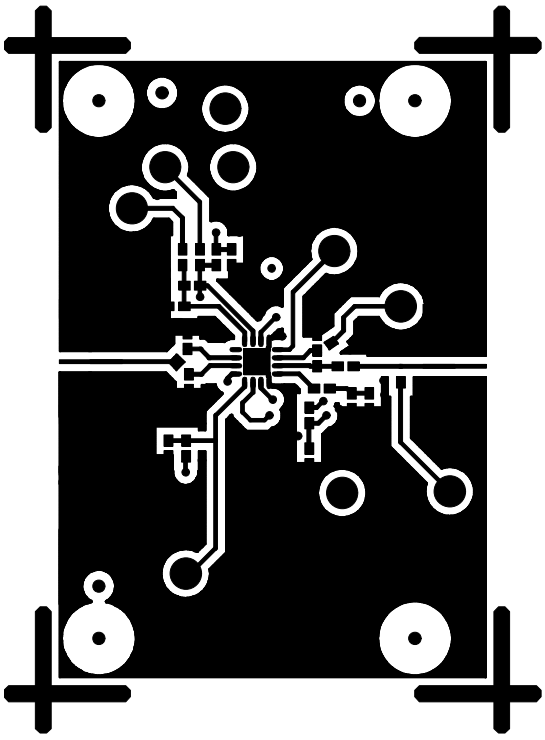


Fig 28 Evaluation Board Layout, Top

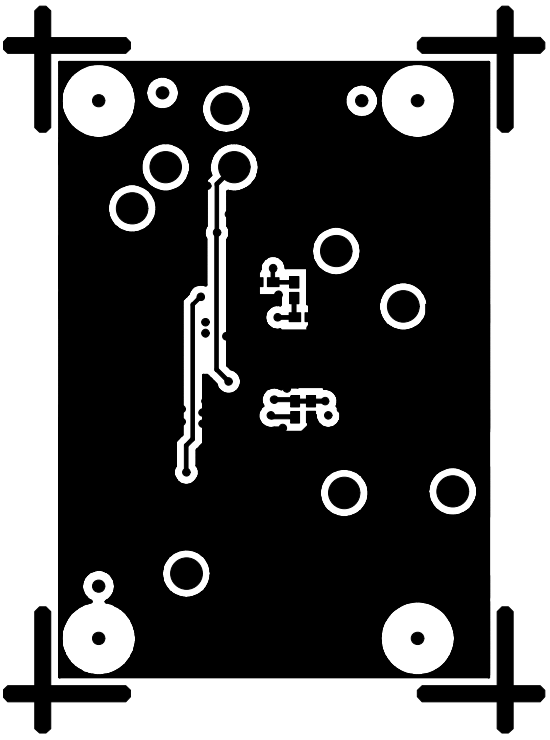


Fig 30 Evaluation Board Layout, Bottom

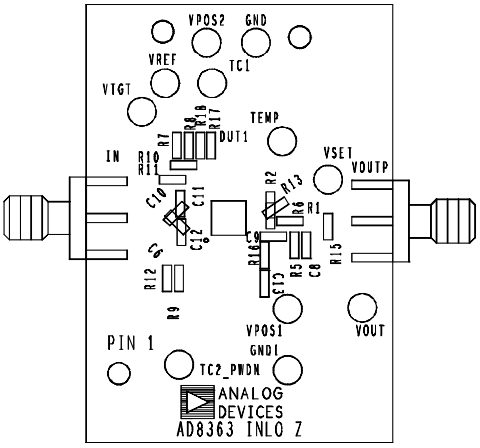


Fig 29 Evaluation Board Assembly, Top

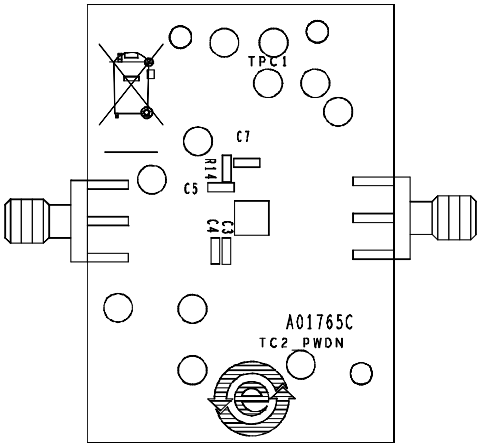
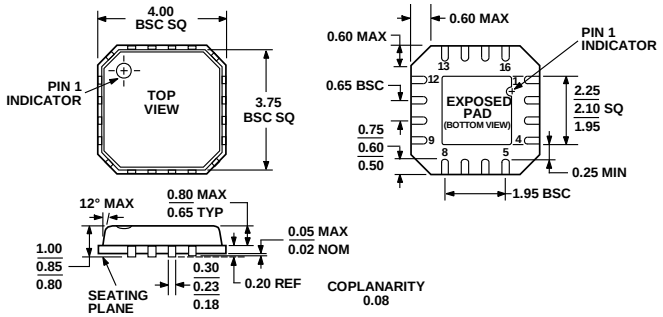


Fig 31 Evaluation Board Assembly, Bottom

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
AD8363ACPZ-R7	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	1500
AD8363ACPZ-R2	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	250
AD8363ACPZ-WP	40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	64
AD8363-EVALZ		Evaluation Board		